

IPCTECH Motherboard User's Manual

QY-MB-1215U-3.5

1. Models and Attentions

1.1 Models

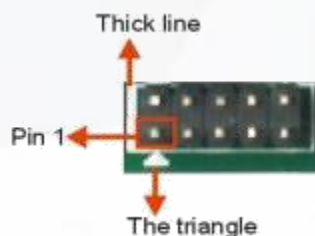
This manual is applied to following models:

Model	CPU	COM	LAN	HDMI	DP++	LVDS/ eDP	USB	M.2 KEY-M	M.2 KEY-E	M.2 KEY-B	SATA 3.0
QY-MB-1215U-3.5	i3-1215U	6	2	1	1	LVDS	9	PCIE 4x	PCIE	PCIE+ USB3.0 +USB2.0	1
	i5-1235U	6	2	1	1	LVDS	9	PCIE 4x	PCIE	PCIE+ USB3.0 +USB2.0	1
	i5-1240P	6	2	1	1	LVDS	9	PCIE 4x	PCIE	PCIE+ USB3.0 +USB2.0	1
	i3-1315U	6	2	1	1	LVDS	9	PCIE 4x	PCIE	PCIE+ USB3.0 +USB2.0	1
	i5-1335U	6	2	1	1	LVDS	9	PCIE 4x	PCIE	PCIE+ USB3.0 +USB2.0	1
	i5-1340P	6	2	1	1	LVDS	9	PCIE 4x	PCIE	PCIE+ USB3.0 +USB2.0	1

1.2 Attentions

- Notes under a table or figure indicate the difference of models, or alternative definition of specific pin of the header (jumper/connector).
- How to identify the first pin of a header or jumper

Usually, there is a thick line or a triangle near the header' s or jumper' s pin 1.



Square pad, which you can find on the back of the motherboard, is usually used for pin 1.



2. Specification

Model		QY-MB-1215U-3.5		
CPU	CPU Model	Intel® Core™ Alder Lake-P Processor		
		i3-1215U	i5-1235U	i5-1240P
	Clock Speed	1.20GHz	1.30GHz	1.70GHz
	Multi-Core	2P4E	2P8E	4P4E
	TDP	15W	15W	28W
	Graphics	Intel® UHD Graphics	Intel® Iris® Xe Graphics	
		Up to 64 EUs, 1.10 GHz	Up to 80 Eus, 1.20 GHz	Up to 80 Eus, 1.30 GHz
Display		1 * HDMI (TYPE-A): max resolution up to 2048*1080@60Hz 1 * DP++ (TYPE-A): max resolution up to 4096*2304@60Hz 1 * LVDS/eDP (Wafer): LVDS max resolution up to 1920*1200@60Hz (Default) or eDP max resolution up to 3840*2160@60Hz		
Memory		Support DDR4-3200 MHz, 1 * non-ECC SO-DIMM Slot, up to 32GB		
Storage		1 * SATA3.0 7P Connector (With 1 * SATA Power Wafer) 1 * M.2 Key-M Slot (PCIe x4/ SATA, Default PCIE 4x, Support PCIe x4 NVMe, 2280)		
Ethernet		2 * Intel® GbE LAN Chip (10/100/1000 Mbps, RJ45)		
Audio		Realtek Audio HAD Codec, 1 * Line-Out + MIC 2in1 3.5mm Jack 1 * Amplifier Wafer, 3-W (per channel) into a 4-Ω Loads		
Expansion Slots		1 * M.2 Key-E Slot (PCIE+USB2.0, Default PCIE, Support WIFI, 2230) [1] 1 * M.2 Key-B Slot (PCIE + USB3.0 + USB2.0, Support 5G/4G, 2242/3052) [2] 1 * SIM Card Wafer		
COM ^[3]		2 * RS232 (COM1/2, Wafer, Full lanes) 3 * RS232/TTL (COM3/4/5, Wafer, 3 lanes) 1 * RS232/RS485/TTL (COM6, Wafer, 3 lanes)		
USB		6 * USB3.0 (TYPE-A, Rear IO) 3 * USB2.0 (Wafer, Internal) ^{[1][2]}		
Other Ports		1 * 8-bit GPIO Wafer 1 * Front Panel Wafer 1 * I2C Touch Wafer 1 * System FAN Wafer 1 * CPU FAN Wafer 1 * CMOS Clear Jumper		

System	Windows 10 IoT Enterprise 2021 LTSC, Windows 10 (21H2), Windows 11 (21H2) or later, Linux Kernel 5.17 or later
Temperature	Storage: -20~75°C Operating: 0~60°C
BIOS	AMI UEFI BIOS (Support Watchdog Timer)
Power Supply	DC12V/24VAuto Detect (DC 24V or 12V Optional) 1 * DC 12V/24V Power Input Φ 2.5mm Thread Jack (2P 3.5mm/5.08mm Terminal Block Optional)
Factor	3.5-inch Standard (146mm * 105mm)

Notes:

[1]: One of USB2.0 signal for M.2_KEYB_SSD/WWAN1 colay with F_USB2. They can' t be used at the same time. (resistor selectable)

[2]: One of USB2.0 signal for M.2_KEYE_WLAN1 colay with F_USB2. They can' t be used at the same time. (resistor selectable)

[3]: TTL signal of COM3/4/5/6 come from the same IC. They must be RS232 or TTL at the same time.

Model		QY-MB-1335U-3.5		
CPU	CPU Model	Intel® Core™ Raptor Lake-P Processor		
		i3-1315U	i5-1335U	i5-1340P
	Clock Speed	1.2 GHz	1.3 GHz	1.9 GHz
	Multi-Core	2P4E	2P8E	4P8E
	TDP	15W	15W	28W
	Graphics	Intel® UHD Graphics	Intel® Iris® Xe Graphics	
		Up to 64 EUs, 1.25 GHz	Up to 80 Eus, 1.25 GHz	Up to 80 Eus, 1.45 GHz
Display		1 * HDMI (TYPE-A): max resolution up to 2048*1080@60Hz 1 * DP++ (TYPE-A): max resolution up to 4096*2304@60Hz 1 * LVDS/eDP (Wafer): LVDS max resolution up to 1920*1200@60Hz (Default) or eDP max resolution up to 3840*2160@60Hz		
Memory		Support DDR4-3200 MHz, 1 * non-ECC SO-DIMM Slot, up to 32GB		
Storage		1 * SATA3.0 7P Connector (With 1 * SATA Power Wafer) 1 * M.2 Key-M Slot (PCIe x4/ SATA, Default PCIE 4x, Support PCIe x4 NVMe, 2280)		
Ethernet		2 * Intel® GbE LAN Chip (10/100/1000 Mbps, RJ45)		
Audio		Realtek Audio HAD Codec, 1 * Line-Out + MIC 2in1 3.5mm Jack 1 * Amplifier Wafer, 3-W (per channel) into a 4-Ω Loads		
Expansion Slots		1 * M.2 Key-E Slot (PCIE+USB2.0, Default PCIE, Support WIFI, 2230) [1] 1 * M.2 Key-B Slot (PCIE + USB3.0 + USB2.0, Support 5G/4G, 2242/3052) [2] 1 * SIM Card Wafer		
COM ^[3]		2 * RS232 (COM1/2, Wafer, Full lanes) 3 * RS232/TTL (COM3/4/5, Wafer, 3 lanes) 1 * RS232/RS485/TTL (COM6, Wafer, 3 lanes)		
USB		6 * USB3.0 (TYPE-A, Rear IO) 3 * USB2.0 (Wafer, Internal) [1][2]		

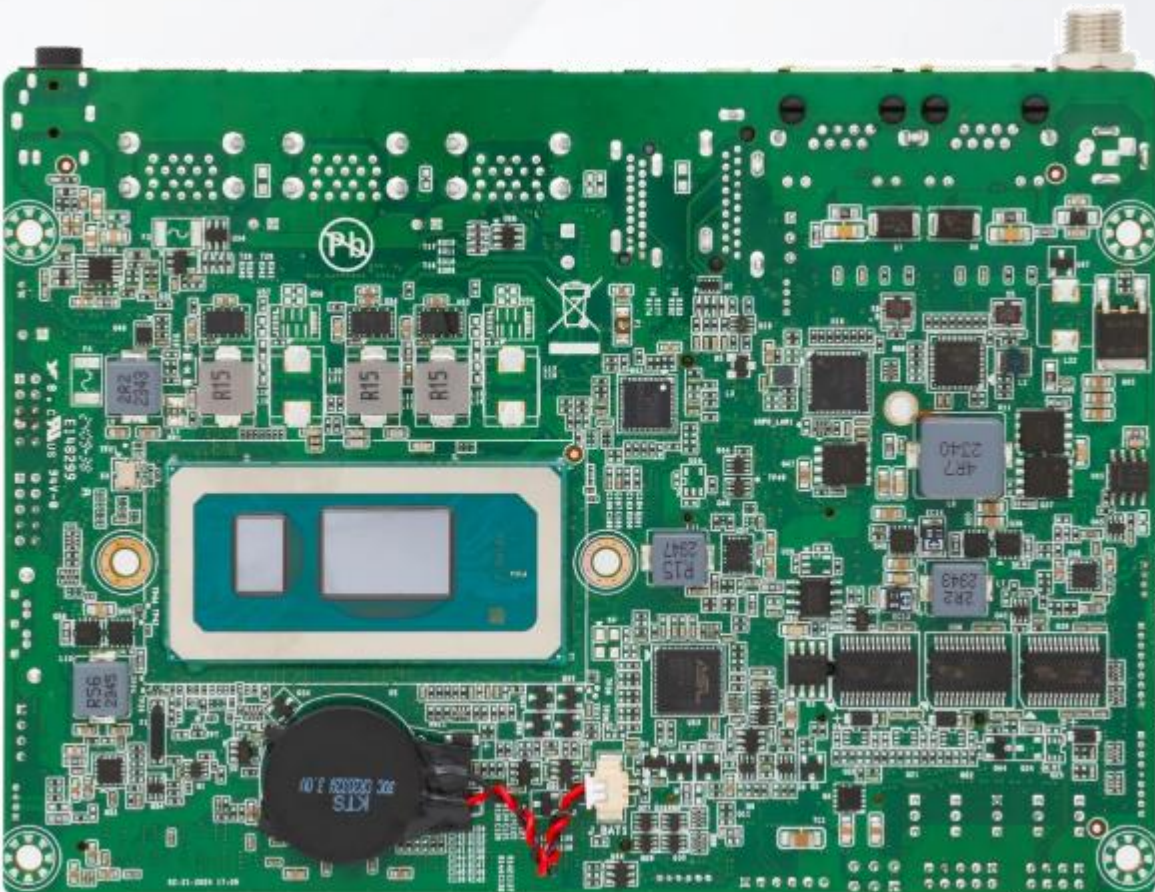
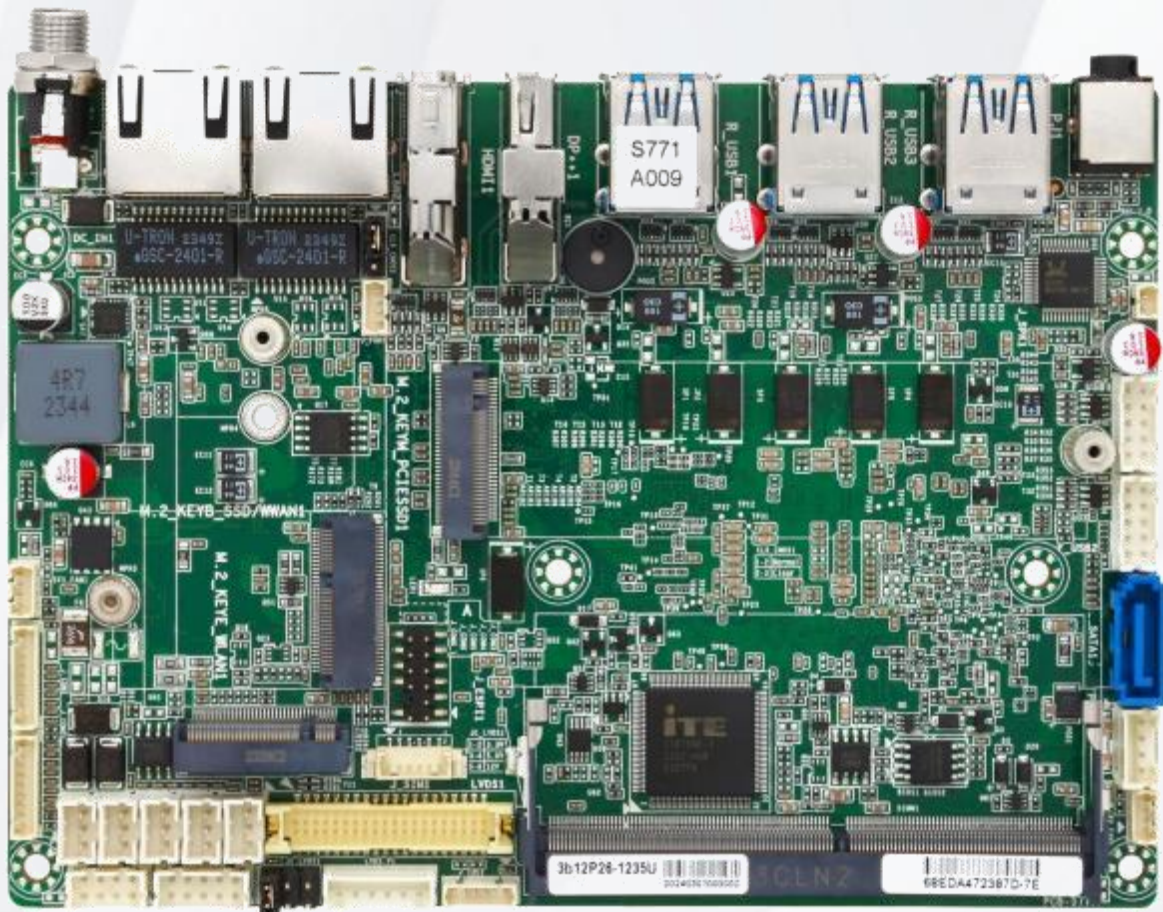
Other Ports	1 * 8-bit GPIO Wafer 1 * Front Panel Wafer 1 * I2C Touch Wafer 1 * System FAN Wafer 1 * CPU FAN Wafer 1 * CMOS Clear Jumper
System	Windows 10 IoT Enterprise 2021 LTSC, Windows 10 (21H2), Windows 11 (21H2) or later, Linux Kernel 5.17 or later
Temperature	Storage: -20~75°C Operating: 0~60°C
BIOS	AMI UEFI BIOS (Support Watchdog Timer)
Power Supply	DC12V/24VAuto Detect (DC 24V or 12V Optional) 1 * DC 12V/24V Power Input Φ 2.5mm Thread Jack (2P 3.5mm/5.08mm Terminal Block Optional)
Factor	3.5-inch Standard (146mm * 105mm)

Notes:

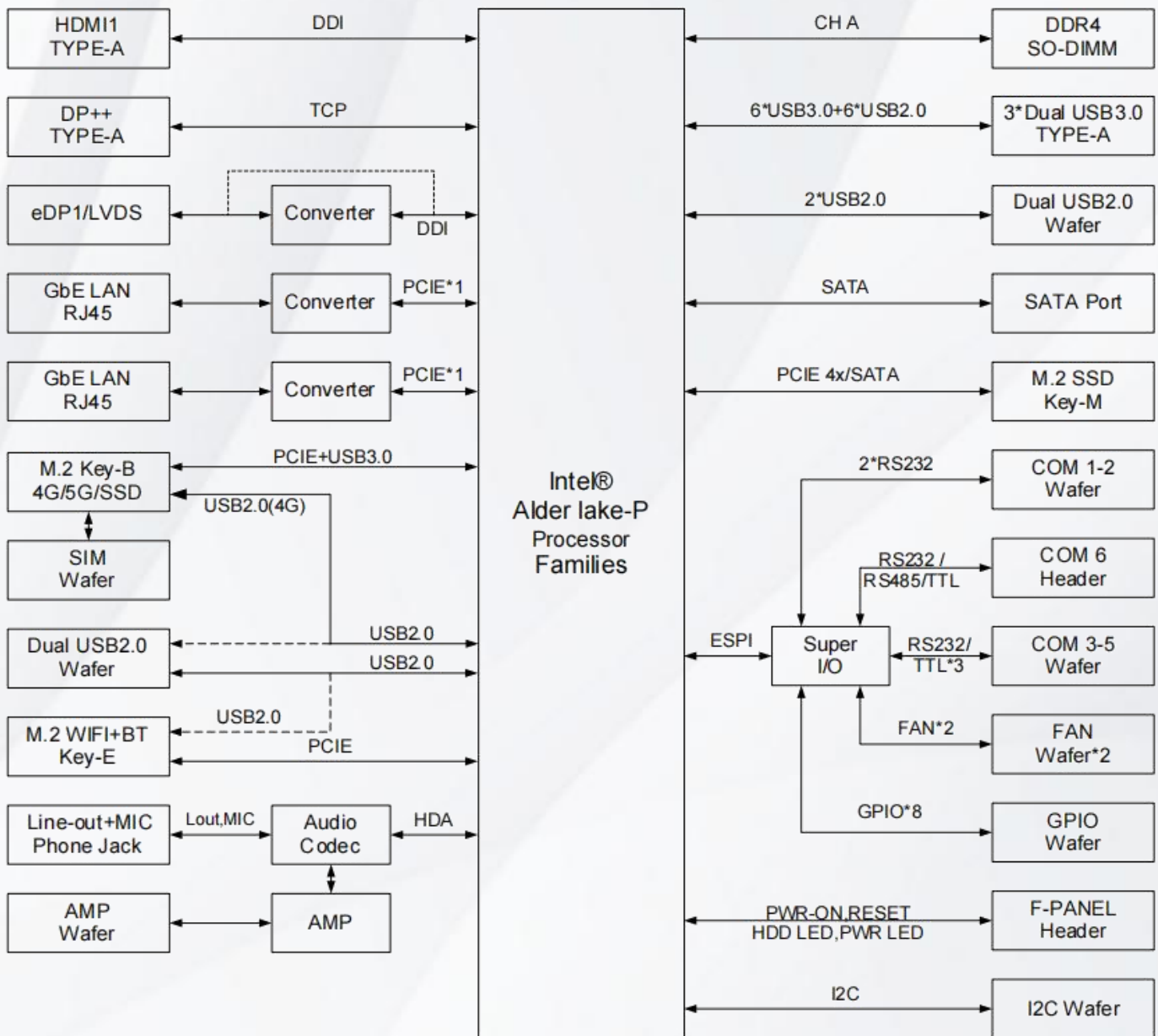
[1]: One of USB2.0 signal for M.2_KEYB_SSD/WWAN1 colay with F_USB2. They can' t be used at the same time. (resistor selectable)

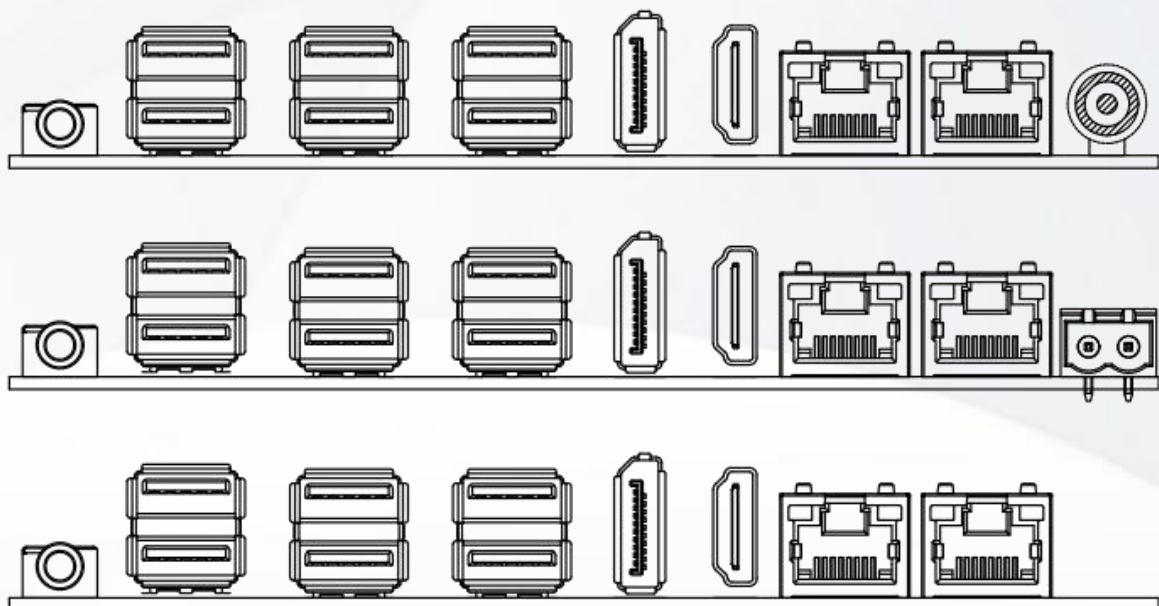
[2]: One of USB2.0 signal for M.2_KEYE_WLAN1 colay with F_USB2. They can' t be used at the same time. (resistor selectable)

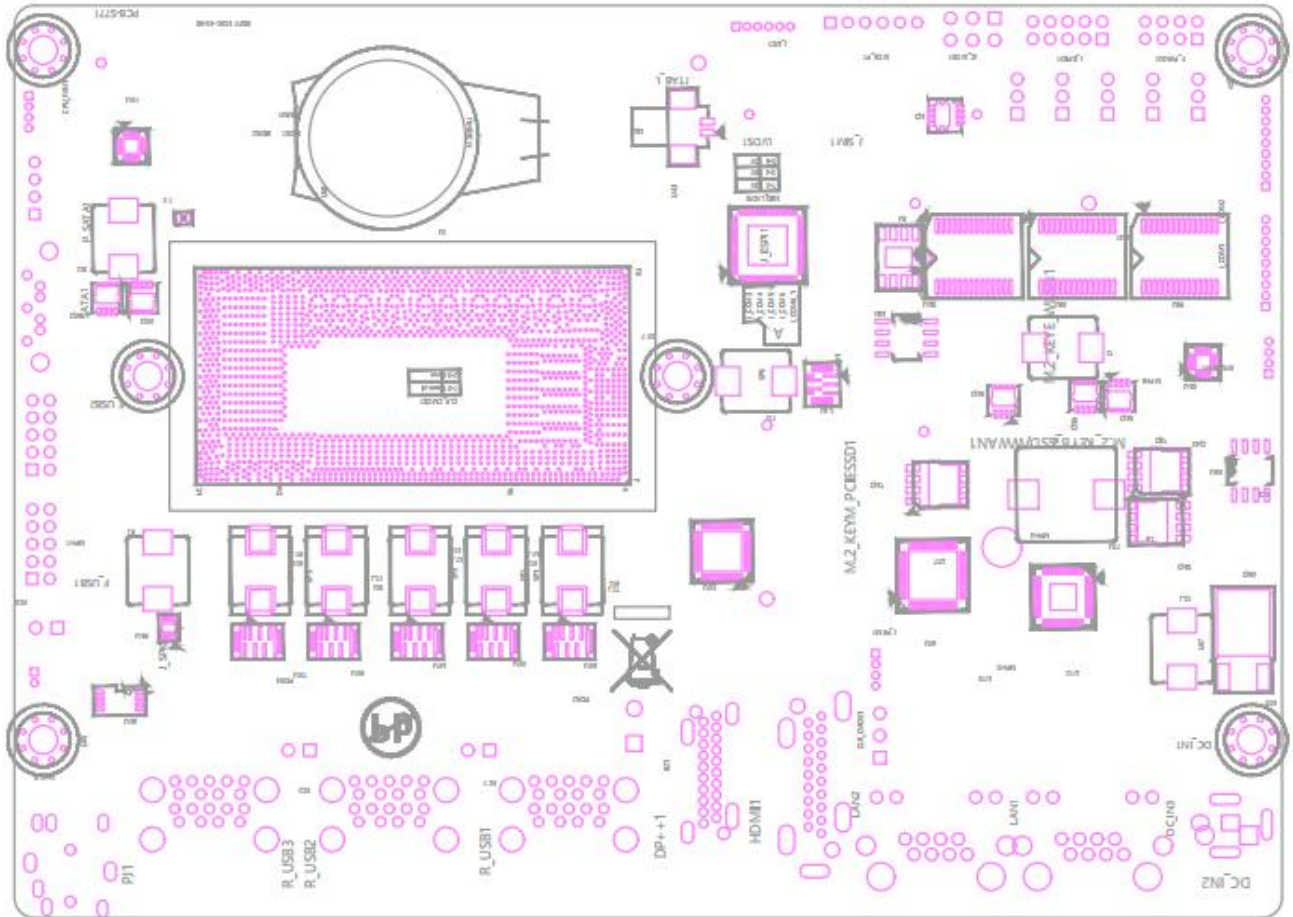
[3]: TTL signal of COM3/4/5/6 come from the same IC. They must be RS232 or TTL at the same time.



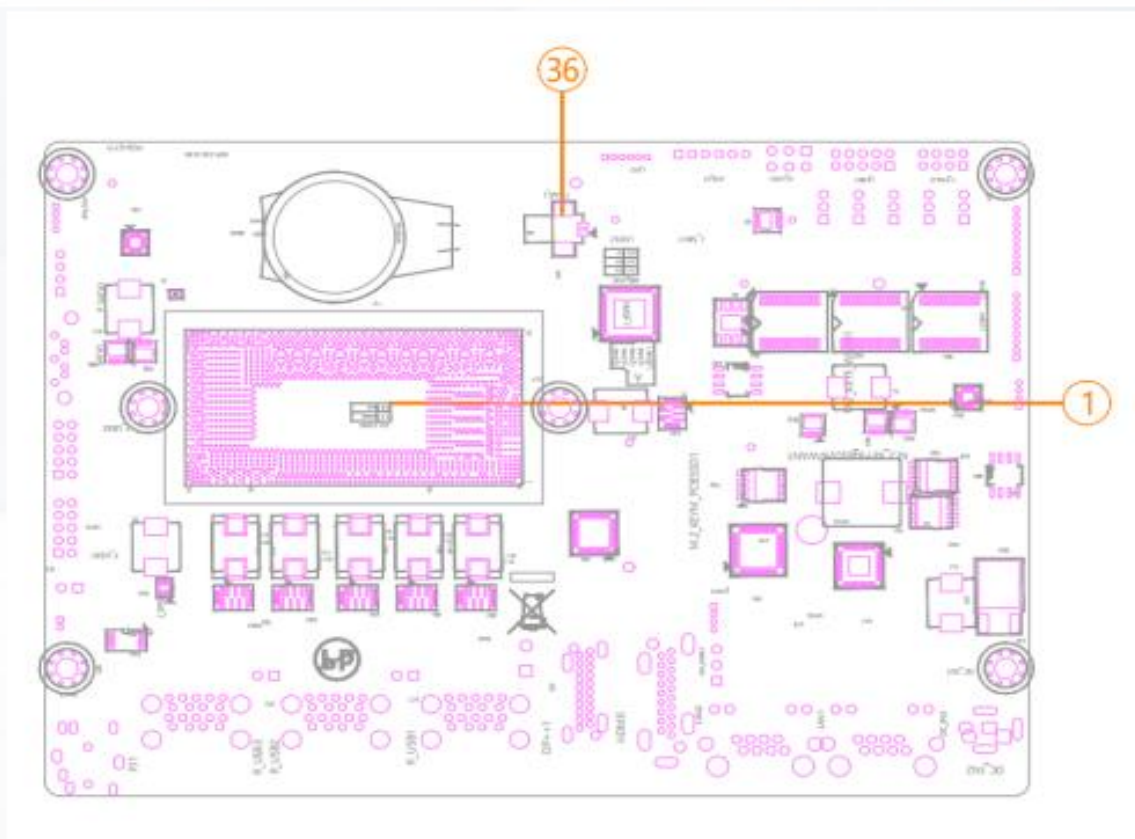
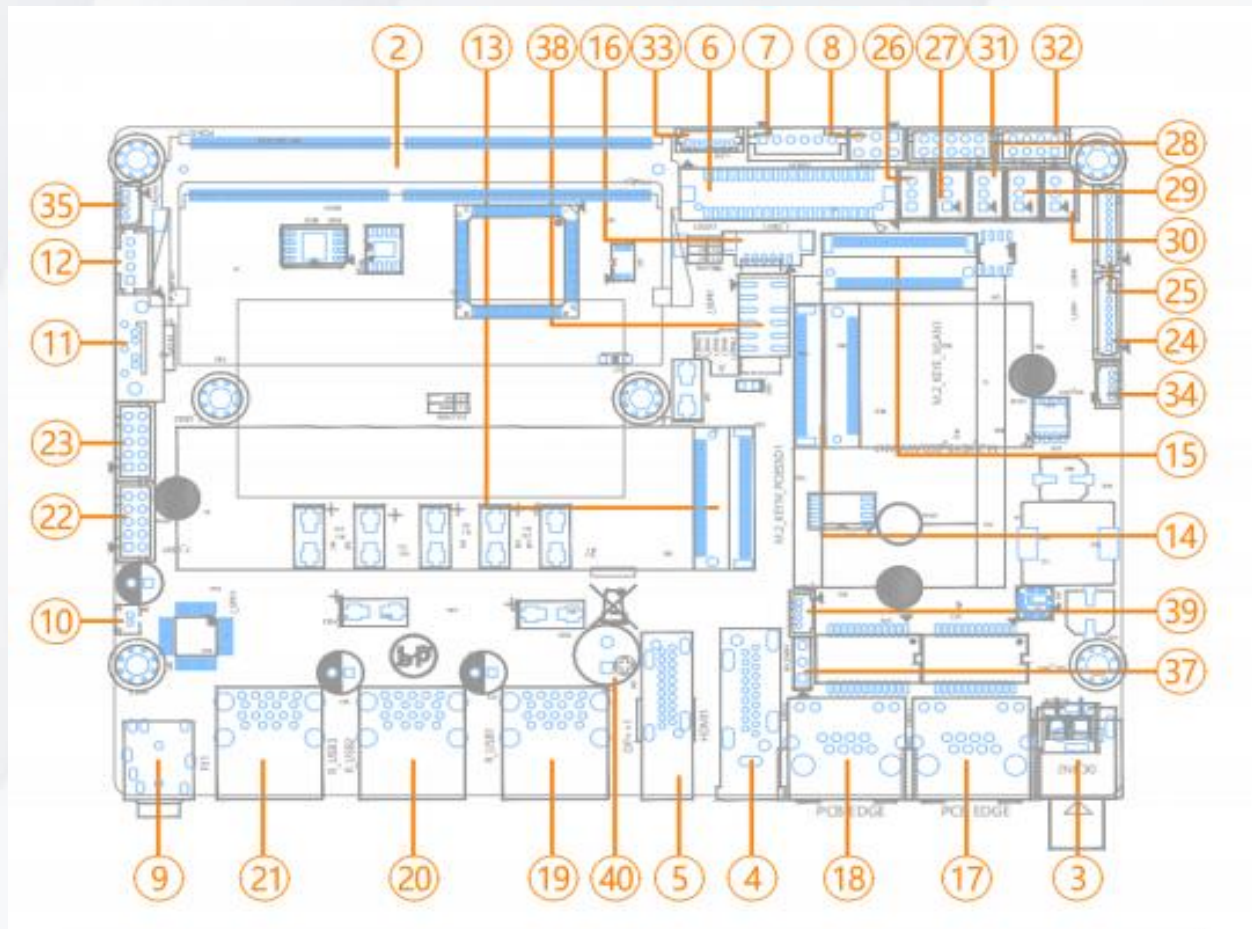
3. Block Diagram







4. Jumper/ Headers and Connectors



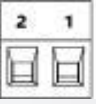
Jumpers / Headers and Connectors

①	U1	CPU
②	DIMM1	DDR4 SO-DIMM Slot
③	DC_IN1 (DC_IN) (DC_IN)	DC Power Input Φ2.5mm Thread Jack (DC Power Input 2P 3.5mm Terminal Block) (DC Power Input 2P 5.08mm Terminal Block)
④	HDMI1	HDMI Upright TYPE-A Connector
⑤	DP++1	DP++ Upright Connector
⑥	LVDS1	eDP/LVDS Signal Wafer
⑦	LVDS_P1	eDP/LVDS Backlight Control Wafer
⑧	JC_LVDS1	eDP/LVDS VDD Select Jumper
⑨	PJ1	Line-Out + MIC 2in1 3.5mm Jack
⑩	J_SPK1	Amplifier Wafer
⑪	SATA1	SATA3.0 7P Connector
⑫	P_SATA1	SATA Power Wafer
⑬	M.2_KEYM_PCIESSD1	M.2 Key-M Slot (PCIe x4/SATA, Support PCIe x4 NVMe/ SATA SSD, 2280)
⑭	M.2_KEYE_WLAN1	M.2 Key-E Slot (PCIe+USB2.0, Support WIFI+ BlueTooth, 2230)
⑮	M.2_KEYB_SSD/WWAN1	M.2 Key-B Slot (PCIe + USB3.0 + USB2.0, Support5G/4G, 2242/3052)
⑯	J_SIM1	SIM Card Wafer
⑰	LAN1	GbE LAN RJ45 Connector
⑱	LAN2	GbE LAN RJ45 Connector
⑲	R_USB1	Dual USB3.0 TYPE-A Connector
⑳	R_USB2	Dual USB3.0 TYPE-A Connector
㉑	R_USB3	Dual USB3.0 TYPE-A Connector
㉒	F_USB1	Front USB2.0 Wafer
㉓	F_USB2	Front USB2.0 Wafer
㉔	J_COM1	COM1 Wafer

②5	J_COM2	COM2 Wafer
②6	J_COM3	COM3 Wafer
②7	J_COM4	COM4 Wafer
②8	J_COM5	COM5 Wafer
②9	J_COM6	COM6 Wafer
③0	J_COM6_1	COM6 RS485 Wafer
③1	J_GPIO1	GPIO Wafer
③2	F_PANEL1	Front Panel Wafer
③3	J_I2C1	I2C Wafer
③4	SYS_FAN1	System FAN Wafer
③5	CPU_FAN1	CPU FAN Wafer
③6	J_BAT1	CMOS Battery Wafer
③7	CLR_CMOS1	CMOS Clear Jumper
③8	J_ESPI1	ESPI Debug Header
③9	J_PRM1	Power Debug Wafer

6. Definition of Jumpers /Headers and Connectors

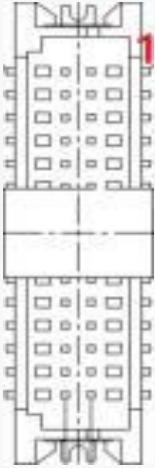
1) Mark No.3 DC_IN2 (DC Power Input 2P Terminal Block 2*1 Pin 3.50 mm)

Graphic	Pin	Definition	Pin	Definition
	1	VCC_IN	2	GN

2) Mark No.3 DC_IN3 (DC Power Input 2P Terminal Block 2*1 Pin 5.08 mm)

Graphic	Pin	Definition	Pin	Definition
	1	VCC_IN	2	GND

3) Mark No.6 LVDS1 (eDP/LVDS Signal Wafer 20*2 Pin 1.25mm)

Graphic	Pin	Definition	Pin	Definition
	1	VDD_PANEL ^[1]	2	VDD_PANEL ^[1]
	3	LVDS_PRSENT	4	GND
	5	VDD_PANEL ^[1]	6	VDD_PANEL ^[1]
	7	LVDS_A_DATA0-	8	LVDS_B_DATA0- /EDP1_TX0- ^[2]
	9	LVDS_A_DATA0+	10	LVDS_B_DATA0+ /EDP1_TX0+ ^[2]
	11	GND	12	GND
	13	LVDS_A_DATA1-	14	LVDS_B_DATA1- /EDP1_TX1- ^[2]
	15	LVDS_A_DATA1+	16	LVDS_B_DATA1+ /EDP1_TX1+ ^[2]
	17	GND	18	GND
	19	LVDS_A_DATA2-	20	LVDS_B_DATA2- /EDP1_TX2-
	21	LVDS_A_DATA2+	22	LVDS_B_DATA2+ /EDP1_TX2+
	23	GND	24	GND
	25	LVDS_A_CLK-	26	LVDS_B_CLK- /EDP1_TX3- ^[2]
	27	LVDS_A_CLK+	28	LVDS_B_CLK+ /EDP1_TX3+ ^[2]
	27	LVDS_A_CLK+	28	LVDS_B_CLK+ /EDP1_TX3+ ^[2]

	29	GND	30	GND
	31	N/C	32	EDP1_HPDC
	33	GND	34	GND
	35	LVDS_A_DATA3-	36	LVDS_B_DATA3- /EDP1_AUX- [2]
	37	LVDS_A_DATA3+	38	LVDS_B_DATA3+ /EDP1_AUX+ [2]

Notes:

[1]: Panel Power VDD is 3.3V by default, 5V or 12V is selectable by "eDP/LVDS VDD Select Jumper" . (JV_LVDS1, Mark 8).

[2]: It supports LVDS by default and can support eDP if specified. (BOM selectable).

4) Mark No.7 LVDS_P1 (eDP/LVDS Backlight Control Wafer 6*1 Pin 2.00mm)

Graphic	Pin	Definition	Pin	Definition
	1	GND	4	LVDS_BKLT_EN
	2	GND	5	VCC12
	3	LVDS_BKLT_CTL	6	VCC12

5) Mark No.8 JC_LVDS1 (eDP/LVDS VDD Select Jumper 3*2 Pin 2.54 mm)

Graphic	Setting	Function
	1-2 (Default)	VCC3.3
	3-4	VCC5
	5-6	VCC12

6) Mark No.10 J_SPK1 (Amplifier Wafer 2*1 Pin 1.25 mm)

Graphic	Pin	Definition	Pin	Definition
	1	SPK_OUT+	2	SPK_OUT-

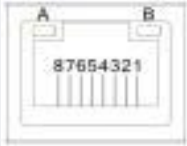
7) Mark No.12 P_SATA1 (SATA Power Wafer 4*1 Pin 2.00 mm)

Graphic	Pin	Definition	Pin	Definition
	1	VCC12	3	GND
	2	GND	4	VCC5

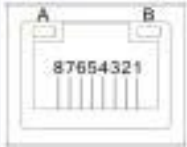
8) Mark No.16 J_SIM1 (SIM Card Wafer 6*1 Pin 1.25mm)

Graphic	Pin	Definition	Pin	Definition
	1	UIM_PWR	4	UIM_CLK
	2	UIM_DATA	5	UIM_RST
	3	GND	6	UIM_VPP

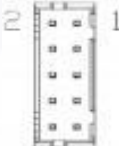
9) Mark No.17 LAN1 (GbE LAN RJ45 Connector)

Graphic	Pin	Definition	Pin	Definition
	1	MDI0+	5	MDI2-
	2	MDI0-	6	MDI1-
	3	MDI1+	7	MDI3+
	4	MDI2+	8	MDI3-
	A	Active LED	B	Speed LED
		ACT: Twinkling Yellow		1000M: Turn Yellow
		Only LINK: Lights On		100M: Turn Green
		Stop: Lights Off		10M: Lights Off

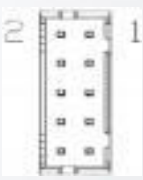
10) Mark No.18 LAN2 (GbE LAN RJ45 Connector)

Graphic	Pin	Definition	Pin	Definition
	1	MDI0+	5	MDI2-
	2	MDI0-	6	MDI1-
	3	MDI1+	7	MDI3+
	4	MDI2+	8	MDI3-
	A	Active LED	B	Speed LED
		ACT: Twinkling Yellow		1000M: Turn Yellow
		Only LINK: Lights On		100M: Turn Green
		Stop: Lights Off		10M: Lights Off

11) Mark No.22 F_USB1 (Front USB2.0 Wafer 5*2 Pin 2.00 mm)

Graphic	Pin	Definition	Pin	Definition
	1	VCC5	2	VCC5
	3	USB2.0_1-	4	USB2.0_2-
	5	USB2.0_1+	6	USB2.0_2+
	7	GND	8	GND
	9	GND	10	GND

12) Mark No.23 F_USB2 (Front USB2.0 Wafer 5*2 Pin 2.00 mm)

Graphic	Pin	Definition	Pin	Definition
	1	VCC5	2	VCC5
	3	USB2.0_1-	4	USB2.0_2-
	5	USB2.0_1+	6	USB2.0_2+
	7	GND	8	GND
	9	GND	10	GND

13) Mark No.24 J_COM1 (COM1 Wafer 9*1 Pin 1.25mm)

Graphic	Pin	Definition	Pin	Definition
	1	PIN1 ^[1]	6	CTS
	2	DSR	7	DTR
	3	RXD	8	PIN9 ^[2]
	4	RTS	9	GND
	5	TXD		

Notes:

[1]: PIN1 can be DCD#/12V SEL by RES, support DCD# by default.

[2]: PIN9 can be RI#/5V SEL by RES, support RI# by default.

14) Mark No.25 J_COM2 (COM2 Wafer 9*1 Pin 1.25mm)

Graphic	Pin	Definition	Pin	Definition
	1	PIN1 ^[1]	6	CTS
	2	DSR	7	DTR
	3	RXD	8	PIN9 ^[2]
	4	RTS	9	GND
	5	TXD		

Notes:

[1]: PIN1 can be DCD#/12V SEL by RES, support DCD# by default.

[2]: PIN9 can be RI#/5V SEL by RES, support RI# by default.

15) Mark No.26 J_COM3 (COM3 Wafer 3*1 Pin 2.00 mm)

Graphic	Pin	Definition	Pin	Definition
	1	RXD	3	GND
	2	TXD		

16) Mark No.27 J_COM4 (COM4 Wafer 3*1 Pin 2.00 mm)

Graphic	Pin	Definition	Pin	Definition
	1	RXD	3	GND
	2	TXD		

17) Mark No.28 J_COM5 (COM5 Wafer 3*1 Pin 2.00 mm)

Graphic	Pin	Definition	Pin	Definition
	1	RXD	3	GND
	2	TXD		

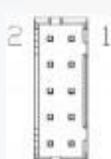
18) Mark No.29 J_COM6 (COM6 Wafer 3*1 Pin 2.00 mm)

Graphic	Pin	Definition	Pin	Definition
	1	RXD	3	GND
	2	TXD		

19) Mark No.30 J_COM6_1 (COM6_1 RS485 Wafer 3*1 Pin 2.00 mm)

Graphic	Pin	Definition	Pin	Definition
	1	RS485+	3	GND
	2	RS485-		

20) Mark No.31 J_GPIO1 (GPIO Wafer 5*2 Pin 2.00 mm)

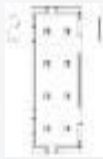
Graphic	Pin	Definition	Pin	Definition
	2	SIO_GPIO70 (0xA06 Bit0, H ^[1])	1	SIO_GPIO71 (0xA06 Bit1, H ^[1])
	4	SIO_GPIO72 (0xA06 Bit2, H ^[1])	3	SIO_GPIO73 (0xA06 Bit3, H ^[1])
	6	SIO_GPIO74 (0xA06 Bit4, H ^[1])	5	SIO_GPIO75 (0xA06 Bit5, H ^[1])
	8	SIO_GPIO76 (0xA06 Bit6, H ^[1])	7	SIO_GPIO77 (0xA06 Bit7, H ^[1])
	10	+3.3V ^[2]	9	GND

Notes:

[1]: "H" or "L" means the default voltage is High or Low level (3.3V GPIO).

[2]: Power on this Pin is 3.3V by default, 5V is available if specified. (resistor selectable)

21) Mark No.32 F_PANEL1 (Front Panel Wafer 4*2 Pin 2.00 mm)

Graphic	Pin	Definition	Pin	Definition
	1	PWR_LED+	2	HDD_LED+
	3	PWR_LED-	4	HDD_LED-
	5	PWR+	6	RESET-
	7	PWR-	8	RESET+

22) Mark No.33 J_I2C1 (I2C Wafer 6*1 Pin 1.25 mm)

Graphic	Pin	Definition	Pin	Definition
	1	VCC3.3	4	RST
	2	GND	5	SCL
	3	INT	6	SDA

23) Mark No.34 SYS_FAN1 (System FAN Wafer 4*1 Pin 1.25 mm)

Graphic	Pin	Definition	Pin	Definition
	1	GND	3	FAN Speed Detection
	2	VCC5 ^[1]	4	FAN Speed Control

Notes:

[1]: Power on this Pin is 5V by default,12V is available if specified. (resistor selectable)

24) Mark No.35 CPU_FAN1 (CPU FAN Wafer 4*1 Pin 1.25 mm)

Graphic	Pin	Definition	Pin	Definition
	1	GND	3	FAN Speed Detection
	2	VCC5 ^[1]	4	FAN Speed Control

Notes:

[1]: Power on this Pin is 5V by default,12V is available if specified. (resistor selectable)

25) Mark No.36 J_BAT1 (CMOS Battery Wafer 2*1 Pin 1.25mm)

Graphic	Pin	Definition	Pin	Definition
	1	VCC_BAT	2	GND

26) Mark No.37 CLR_CMOS1 (CMOS Clear Jumper 3*1 Pin 2.54 mm)

Graphic	Setting	Function
	1-2(Default)	Normal
	2-3	Clear CMOS

27) Mark No.38 J_ESPI1 (ESPI Debug Header 6*2 Pin 2.00 mm)

Graphic	Pin	Definition	Pin	Definition
	1	ESPI_IO0	2	VCC3.3
	3	ESPI_IO1		
	5	ESPI_IO2	6	ESPI_CLK
	7	ESPI_IO3	8	GND
	9	ESPI_CS0-	10	VCC3.3
	11	ESPI_ALERT0_N	12	PLTRST_N ^[1]

Notes:

[1]: Signal on this Pin is PLT_RST_N by default, ESPI_RST0_N is available if specified. (resistor selectable) .

28) Mark No.39 J_PRM1 (Power Debug Wafer 4*1 Pin 1.25 mm)

Graphic	Pin	Definition	Pin	Definition
	1	GND	3	VCCIN_SCL
	2	VCCIN_PE	4	VCCIN_SDA

[END]